

Government College of Engineering, Aurangabad
(An Autonomous Institute of Government of Maharashtra)
T.E(Electronics & Telecommunication) End Semester Examination November 2016
ET 342: MICROPROCESSORS AND PERIPHERALS

Time: Three Hours

Date: 15 NOV 2016

Max. Marks. 60

"Verify the course code and check whether you have got the correct question paper"

N.B:- 1. Attempt any SIX questions

2. Figure to the right indicates full marks

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- Q. No. 1** Explain in detail the Von Neumann and Harvard architecture of microprocessor system. What type of architecture is used in 8085 microprocessors? (10)
- Q. No. 2** Draw the functional block diagram of 8085 microprocessor. Draw the circuit diagram of 8085 microcomputer system with all necessary signals for interfacing with peripheral and I/O devices. (10)
- Q. No.3** Explain different addressing modes of 8085 explain with suitable example. Explain branching instructions of 8085 in detail with suitable examples. (10)
- Q. No. 4** Write an assembly language subroutine to transfer a block of memory whose starting address is given in register pair DE to destination address specified in Reg. pair HL and the number of bytes specified in register pair BC. Also show the use of this subroutine in main program. (10)
- Q. No. 5** Draw the timing diagram for execution of interrupt on INTR pin. (10)
- Q. No. 6** Explain in detail how serial data communication is implemented using 8085. Write a program to output serial data through SOD pin. (10)
- Q. No. 7** Draw the circuit to interface 8255 PPI to 8085 microprocessor with Port A address of 8000H. Write a program to initialize 8255 in Mode 1. Explain how data transfer with handshaking signals can be implemented using port C. (10)
- Q. No. 8** Draw the functional block diagram of 8259 programmable interrupt controller and explain the working. (10)
- Q. No.9** Draw the circuit to interface stepper motor using 8255 to 8085 microprocessor. (10)
- Q. No. 10** Draw the functional Pin diagram of 8086 microprocessor. Explain various segment registers and memory segmentation. (10)