# **Electronics & Telecommunication Engineering Department**

**Curriculum: T Y (E&TC)** 

### Government College of Engineering, Aurangabad (An Autonomous Institute)

Teaching and Evaluation Scheme from year 2023-24

Third Year - B. Tech. Program in Electronics & Telecommunication Engineering

Semester	V
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		Cour	20	Too	hing	•	Continu	one Eve	luction	in torma	of Mo	nlza
Course					mo		Conunu	ous Eva	luation	in terms	or wra	IKS
Sr	Cotogor	Course	Course Nome	ти		DD	Cradita	ISE I	ICEI	ISEII	FS	Total
No	v	Code	Course Maine	111	1	IN	Creans	ISE I	ISEI	T	E	(100)
110	3	Coue							-	•		(100)
1	DCC	ETDC2017	Electromagnetic	2			2	15	15	10	60	100
1	PCC	EIPC3017	Engineering	3	-	-	3	15	15	10	00	100
2	PCC	ETPC3018	DigitalSignalProcessing	3	-	-	3	15	15	10	60	100
3	PCC	ETPC3020	Digital Communication	3	-	-	3	15	15	10	60	100
4	PCC	ETPC3022	Embedded Systems	3	-	-	3	15	15	10	60	100
5	PCC	ETPC3019	Lab-Digital Signal Processing	-	-	2	1	-	-	25	25	50
6	PCC	ETPC3021	Lab-Digital Communication	-	-	2	1	-	-	25	25	50
7	PCC	ETPC3023	Lab-Embedded Systems	-	-	2	1	-	-	25	25	50
8	PROJ	ETPR3001	Mini-Project I	-	-	2	1	-	-	25	25	50
9	HSMC II			3	-	-	3	15	15	10	60	100
10	OEC II			3	-	-	3	15	15	10	60	100
11	PEC I*		MOOC/NPTEL Course	3	-	-	3	15	15	10	60	100
			Total	21	-	08	25	105	105	170	520	900
				Seme	ster \	VI						
Sr	Catego	Course	Course Name	TH	Т	PR	Credits	ISE I	ISEII	ISEIII	ESE	Total
No	ry	Code										(100)
1	PCC	ETPC3024	Computer Network	3	-	-	3	15	15	10	60	100
2	PCC	ETPC3025	A.I. and M.L.	3	-	-	3	15	15	10	60	100
3	PEC II			2	-	-	2	15	-	10	50	75
4	PEC III			2	-	-	2	15	-	10	50	75
5	PCC	ETPC3026	Lab-Computer Network & AI & ML	-	-	2	1	-	-	25	-	25
7	PEC II		Lab – PEC II	-	-	2	1	-	-	25	-	25
8	PEC III		Lab – PEC III	-	-	2	1	-	-	25	-	25
9	PROJ	ETPR3002	Mini-Project II	-	-	2	1	-	-	25	25	50
10	OEC III			3	-	-	3	15	15	10	60	100
11	HSMC III			3	-	-	3	15	15	10	60	100
12	HSMC			3	-	-	3	15	15	10	60	100
	1 V	1	Total	19	-	08	23	105	75	170	425	775

Industrial training of a minimum of 4 weeks may be completed after the second/third year, Activities from Group I and Group II may be completed this year which needs to be registered in 8<sup>th</sup> semester.

\*This is MOOC/NPTEL course. Students have to register and appear for the assignments and examination conducted by MOOC/NPTEL course only. After submitting the Passing certificate of such course, students will be awarded the 3 credits by virtue of 'Transfer of Credits'.

Approved in XXV<sup>th</sup> Academic Council Dated: 18<sup>th</sup> April 2023

Professional	Sr.	Course	Course Title
Elective	No.	Code	
Ι	01	ETPE3001	Computer Architecture
(MOOC/	02	ETPE3002	Operating System Fundamentals
NPTEL	03	ETPE3003	Quantum Computing
Courses)	04	ETPE3004	Any other MOOC/NPTEL course on current technology
(3+0+0)		onwards	with the permission of BoS Chairman
II	01	ETPE3011	Information Theory and Coding
(2+0+1)	02	ETPE3012	Lab - Information Theory and Coding
	03	ETPE3013	Optical Fiber Communication
	04	ETPE3014	Lab - Optical Fiber Communication
	05	ETPE3015	Microwave Engineering
	06	ETPE3016	Lab - Microwave Engineering
III	01	ETPE3021	Digital Image Processing
(2+0+1)	02	ETPE3022	Lab - Digital Image Processing
	03	ETPE3023	Power Electronics
	04	ETPE3024	Lab - Power Electronics
	05	ETPE3025	Digital System Design
	06	ETPE3026	Lab - Digital System Design
	07	ETPE3027	Industrial Automation
	08	ETPE3028	Lab - Industrial Automation

# **List of Professional Elective Courses**

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Approved in XXV<sup>th</sup> Academic Council Dated: 18<sup>th</sup> April 2023

ETPC3017: Electromagnetic Engineering				
Teaching Scheme	Examination Scheme			
Lectures: 3 Hrs/Week	ISE I : 15 Marks			
	ISE II:15 Marks			
Total Credits: 03	ISE III: 10 Marks			
	End Semester Exam: 60 Marks			

### **Course Objectives:**

- To understand the three-dimensional representation of vector fields and vector calculus. To understand basic laws of electromagnetics
- To understand the Maxwell's equations as applied to static and time varying fields.
- To understand Transmission lines
- To understand complex electromagnetic phenomenon of wave propagation and electromagnetic radiation & Antenna Fundamentals

Course Outcomes: After completing the course, students will be able to:

CO1	Gain knowledge of coordinate systems & Understand Basic of Electromagnetics
CO2	Understand the Maxwell's equations
CO3	Carryout Impedance transformation Transmission lines (TL) & TL sections for realizing circuit element
CO4	Characterize wave propagation, understanding Plane wave properties
CO5	Understand the phenomenon of wave propagation and electromagnetic radiation.
CO6	Understand Antenna fundamentals.

### **Detailed Syllabus:**

Unit	Electrostatics & Magnetostatics
1	Basic of vector calculus, Electric field intensity, Electric flux density and Divergence,
	Gauss's law, Application of Gauss's Law: Some symmetrical charge distributions,
	Differential volume element, Divergence. Steady magnetic field, Faraday's law, Ampere's
	Circuital law, Curl, Magnetic flux.
Unit	Time Varying Fields and Maxwell's Equations
2	Magnetic boundary conditions, Magnetic Circuit, Potential energy and forces on magnetic
	materials, Displacement current, Maxwell's equations in point form, Maxwell's equations in
	integral form.
Unit	Transmission Lines
3	Equations of Voltage and Current on TX line, Propagation constant and characteristic impedance, and reflection coefficient and VSWR, Impedance Transformation on Loss-less and Low loss Transmission line, Power transfer on TX line, Smith Chart, Admittance Smith Chart, Applications of transmission lines: Impedance Matching, use transmission
	line sections as circuit elements.
Unit	Wave Propagation
4	Wave equation, Poynting vector.Plane waves and properties: reflection and
	refraction, polarization, phase and group velocity, propagation through various media, Wave
	propagation in parallel plane waveguide, rectangular waveguide, skin depth.

#### Unit Antenna Fundamentals

5 Antenna parameters, Isotropic radiators, Radiation power density, Radiation intensity, Directivity (D), Front to back ratio, Antenna bandwidth and Antenna beam width.Rectangular and circular waveguides, dipole and monopole antennas, linear antenna arrays.

Mapping of Course outcome with Program Outcomes and Program Specific Outcome

Course	PO	PO2	PO3	PO	PO	PO	PO	РО	PO	PO	РО	PO	PSO	PSO	PSO
Outcome	1			4	5	6	7	8	9	10	11	12	1	2	3
CO1	3	2								2				3	2
CO2	2	2	1							2		3		3	2
CO3	2									2		3		3	2
CO4	2	2								2				3	2
CO5	2		1	1					3	2				3	2
CO6	2		1							2		3		3	2
		3 – ]	High	1	2 - 1	Mediu	ım 1-	Low							

Assessment:

ISE I:	Shall be based on Class Tests/ Assignments/ Quizzes/ Field visits/ Presentations/ Course Projects
ISE II:	Shall be based on class test
ISE III:	Shall be based on Class Tests/ Assignments/ Quizzes/ Field visits/ Presentations/ Course Projects

#### **Assessment Pattern**

Assessment Pattern Level No.	Knowledge Level	ISEI	ISE II	ISE III	End Semester Examination
K1	Remember	10	00	00	15
K2	Understand	05	10	10	35
K3	Apply	00	05	00	10
K4	Analyze	00	00	00	00
K5	Evaluate	00	00	00	00
K6	Create	00	00	00	00
Total Marks 100		15	15	10	60

#### Assessment table

Assessment Tool	K1	K2	K2	K3	K2
	CO1	CO2	CO3	<b>CO4</b>	CO5
ISE I (15 Marks)	05	10	00	00	00
ISE II (15 Marks)	00	00	10	05	00
ISE III (10 Marks)	00	00	00	00	10
ESE Assessment(60 Marks)	15	10	15	10	10

Approved in XXV<sup>th</sup> Academic Council Dated: 18<sup>th</sup> April 2023

ETPC3018: Digital Signal Processing				
Teaching Scheme	Examination Scheme			
Lectures: 3 Hrs/Week	ISE I:15 Marks			
Credits: 03	ISE II:15 Marks			
	ISE III: 10 Marks			
	End Semester Exam: 60 Marks			

#### **Course description:**

The course covers theory and methods for digital signal processing including basic principles governing the analysis and design of discrete time systems as signal processing devices.

- The primary objective of this course is to provide a thorough understanding and working knowledge of design, implementation, and analysis DSP systems.
- This course in digital signal processing develops essential analysis and design techniques required for a broad range of disciplines.
- Student familiar with most important methods in DSP, including digital filter design, transform domain processing and importance of signal processor.
- After completion of the subject, the student should be able to understand the design principles and the implementation of digital filters and DFT/FFT, and be able to make use of signal processing concepts and wavelets to perform some simple applications.

#### **Course Outcomes**

After completing the course, students will be able to:

COl	Interpret, represent and process discrete/digital signals and systems
CO2	Implement frequency domain analysis of discrete time signals of DSP system
CO3	Understand transforms of signals and systems.
CO4	Design and implement digital filters for processing discrete time signals.
CO5	Develop creative and innovative design that achieves desirable performance criteria within specified objectives and constraints for lifelong learning and continuing professional education.
CO6	Understand the theory of DSP processors with programming skills.

# **Detailed Syllabus**

Unit	Discrete-time Systems and General Realization Techniques										
1	Concept of discrete-time signal. Sampling and reconstruction of signal. Time invariance,										
	causality, linearity, periodic, energy, power convolution and LTI systems										
Unit	Discrete Time Fourier Transform (DTFT):										
2	Concept of frequency in discrete and continuous domain, frequency response in the										
	discrete domain.										
	Z- Transforms:										
	Definition, unit circle, convergence and ROC, properties of Z-transform, characteristic of										
	signals, initial value theorem, Parseval's relation, inverse Ztransform.										
	Discrete Fourier Transform:										
	Relation between DTFT & DFT. Twiddle factors and their properties, computation by										
	different methods, filtering of long data sequences										

	Fast Fourier Transforms:										
	Radix-2 algorithm, decimation-in-time, decimation-in-frequency algorithm, signal flow										
	graph, Butterflies, computations in one place, bit reversal										
	Introduction to Wavelet Transforms										
Unit	Design of Infinite Impulse Response Filters										
3	Revision of analog systems, Butterworth filters and Chebyshev filters. Types of digital										
	filters: IIR and FIR. IIR filter design, bilinear transformation, frequency scaling,										
	transformation from prototype low-pass filter to high-pass filter and band-pass filter.										
	Impulse-invariant and/or step-invariant approaches										
Unit	Design of Finite Impulse Response Filters										
4	FIR filter analysis, Fourier series approach, windowing, Gibbs phenomenon, commonly										
	used windows, concept of linear phase, frequency transformation, low-pass, band-pass,										
	high-pass filters and filter band design.										
Unit	Digital Signal Processors and Applications										
Unit 5	<b>Digital Signal Processors and Applications</b> 1. Architectures and important instruction sets of TMS320c 5416/6713										
Unit 5	<ul> <li>Digital Signal Processors and Applications</li> <li>1. Architectures and important instruction sets of TMS320c 5416/6713</li> <li>2. FPGA: Architecture, different subsystem, design flow of DSP system design, mapping</li> </ul>										
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Unit 5 TEXT 1. 2. 3. 4.	<ul> <li>Digital Signal Processors and Applications <ol> <li>Architectures and important instruction sets of TMS320c 5416/6713</li> <li>FPGA: Architecture, different subsystem, design flow of DSP system design, mapping into DSP algorithm into FPGA.</li> </ol> </li> <li>AND REFERENCE BOOKS <ol> <li>V. Oppenheim and Schafer, Discrete Time Signal Processing, Prentice Hall, 1989.</li> <li>L.R. Rabiner and B. Gold, Theory and Application of Digital Signal Processing, Prentice Hall, 1992.</li> <li>J.R. Johnson, Introduction to Digital Signal Processing, Prentice Hall, 1992.</li> <li>D. J. DeFatta, J. G. Lucas and W. S. Hodgkis, Digital Signal Processing Wiley and Sons,</li> </ol> </li> </ul>										
Unit 5 TEXT 1. 2. 3. 4.	<ul> <li>Digital Signal Processors and Applications <ol> <li>Architectures and important instruction sets of TMS320c 5416/6713</li> <li>FPGA: Architecture, different subsystem, design flow of DSP system design, mapping into DSP algorithm into FPGA.</li> </ol> </li> <li>AND REFERENCE BOOKS <ol> <li>V. Oppenheim and Schafer, Discrete Time Signal Processing, Prentice Hall, 1989.</li> <li>L.R. Rabiner and B. Gold, Theory and Application of Digital Signal Processing, Prentice Hall, 1992.</li> <li>J.R. Johnson, Introduction to Digital Signal Processing, Prentice Hall, 1992.</li> <li>D. J. DeFatta, J. G. Lucas and W. S. Hodgkis, Digital Signal Processing Wiley and Sons, Singapore, 1988.</li> </ol> </li> </ul>										
Unit 5 TEXT 1. 2. 3. 4. 5.	<ul> <li>Digital Signal Processors and Applications <ol> <li>Architectures and important instruction sets of TMS320c 5416/6713</li> <li>FPGA: Architecture, different subsystem, design flow of DSP system design, mapping into DSP algorithm into FPGA.</li> </ol> </li> <li>AND REFERENCE BOOKS <ol> <li>A.V. Oppenheim and Schafer, Discrete Time Signal Processing, Prentice Hall, 1989.</li> <li>L.R. Rabiner and B. Gold, Theory and Application of Digital Signal Processing, Prentice Hall, 1992.</li> <li>J.R. Johnson, Introduction to Digital Signal Processing, Prentice Hall, 1992.</li> <li>D. J. DeFatta, J. G. Lucas and W. S. Hodgkis, Digital Signal Processing Wiley and Sons, Singapore, 1988.</li> <li>Proakis and D.G. Manolakis, 'Digital Signal Processing Principles, Algorithms and</li> </ol> </li> </ul>										
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6. 6. K. Mitra, 'Digital Signal Processing – A Computer Based Approach, Tata McGraw Hill, New Delhi, 2001

# Mapping of Course outcome with Program Outcomes

Course Outcome	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	1	2	1	2	2	-	-	2	2	2	-	-		-	3
CO2	2	1	1	2	2	1	1	2	2	2	-	-		1	3
CO3	2	1	1	1	-	-	1	2	2	1	-	-		1	3
CO4	1	1	1	1	1	1	-	1	1	1	-	1		1	3
CO5	1	2	3	2	1	2	2	1		1	1	1	1	1	3
CO6	2	2	2	1	-	2	1	1		1	1	3	1	1	3

3 – High2 – Medium1 – Low

#### Assessment:

ISE I:	Shall be based on Class Tests/ Assignments/ Quizzes/ Field visits/ Presentations/ Course Projects	
ISE II:	Shall be based on class test	

ISE III:	Shall be based on Class Tests/ Assignments/ Quizzes/ Field visits/ Presentations/ Course
	Projects

### **Assessment Pattern**

Assessment	Knowledge	ISE I	ISE II	ISE III	End
Pattern Level	Level				Semester
No.					Examination
K1	Remember	05	00	00	06
K2	Understand	10	10	05	42
K3	Apply	00	05	05	12
K4	Analyze	00	00	00	00
K5	Evaluate	00	00	00	00
K6	Create	00	00	00	00
Total Marks 1	00	15	15	10	60

# Assessment table

Assessment Tool	K1	K2	K3	K2	K2	K2
	C01	C02	C03	CO4	CO5	CO6
ISE I (15 Marks)	05	10	00	00	00	00
ISE II (15 Marks)	00	00	05	10	00	00
ISE III (10 Marks)	00	00	05	05	00	00
ESE Assessment (60 Marks)	06	12	10	12	12	08

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ETPC3019: Lab-Digital Signal Processing										
Teaching Scheme	Examination Scheme									
Practical: 2 Hrs/Week	ISE III: 25 Marks									
Credits: 01	End Semester Examination: 25 Marks									

### **Purpose:**

The Digital Signal Processing Lab (DSPLAB) provides all the required equipment to implement real-time digital signal processing solutions supporting experimental research, applied research, and industrial projects.

Students simulate the number of experiments in MATLAB. Students also use TMS 320C5416 fixedpoint DSP processors. Programing of the DSP chip is done in C(and some assembly) language using the Code Composer Studio integrated development environment.

Equipment: DSP prototype board or FPGA development tools and platforms, Texas Instruments C6727 Floating Point DSP developer kit.

# Laboratory Course Outcomes

As an outcome of completing the Laboratory course using MATLAB/CCS/IDE, students will be able to:

CO1	The student will be able to carry out simulation of DSP systems.												
CO2	Develop and Implement DSP algorithms in software using a computer language such as C/MATLAB /TMS320C6713 floating point Processor.												
CO3	Analyze Character	and ristics)	Observe of digital I	Magnitude FIR filters.	and	phase	characteristics	(Frequency	response				
CO4	Analyze Character	and ristics)	Observe of digital l	Magnitude IIR filters.	and	phase	characteristics	(Frequency	response				

# List of Experiments

The practical part of the work consists of a minimum of eight tasks that should be performed on the RPi /DSP starter board /or MATLAB simulations.

Sr. No	Details	
1	Program for Discrete-time signals and systems, linear coefficients realization structures, convolution, and correlation using MATLAB	difference equations and
2	Program for DTFT and DFT Spectral Analysis	
3	Program for FFT and Bit reversal	
4	Design and implement of FIR filter, FIR filtering interfacing MATI Studio	AB and Code Composer
5	Design discrete-time digital filters and implement them in real time.	
5	Design and implement of IIR filter	
7	Program for Multi-rate Signal Processing Basic Sampling Rate Alteration Devices • Decimator and Interpolator Design and Implementation	
	<ul><li>Design of Filter Banks</li><li>Design of Nyquist Filters</li></ul>	Annroved in XXV <sup>th</sup> Academic
8	Program for STFT Implementation	Dated: 18th April 2023

9	Introduction to Hardware and Software Tools for the TMS320C6748 Board											
	1. C6000 instruction set architecture or											
	2. Developer Kit (LCDK)											
	3. Or FPGA /Raspberry Pi 3											
	4. TI Code Composer Studio software tools											
	5. TI DSP BIOS (operating system)											
	6. LabVIEW and Matlab											
10	Generating a Sine Wave Using the Hardware and Software Tools for the TI TMS320C6711											
	DSP Processor											

# Mapping of Course outcome with Program Outcomes

Course Outo	come	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1		2	3		3											3
CO2			3		2										1	3
CO3		2	2		1										1	3
CO4					1		1					1			1	3
CO5		2	1			1								1	1	3
CO6				1			2	2						1	1	3

3 – High2 – Medium1 – Low

# **Assessment Table**

Assessment Tool	S2	<b>S</b> 1	S4	S3	S2	S3
	CO1	CO2	CO3	C04	CO5	CO6
ISE III (25 Marks)	05	04	02	05	05	04
Practical Examination & Viva Voce (25 Marks)	05	02	02	10	03	03

#### **Assessment Pattern**

Assessment Pattern Level No.	Skill Level	Term Work	Practical Examination & viva voce
S1	Imitation	08	08
S2	Manipulation	05	05
S3	Precision	10	10
S4	Articulation	02	02
S5	Naturalization	00	00
Total	·	25	25

Approved in XXV<sup>th</sup> Academic Council Dated: 18<sup>th</sup> April 2023

ET	PC3020: Digital Communication	on
Teaching Scheme	Examination Sche	eme
Lectures:3 Hrs/Week	ISE I:	15 Marks
Total Credits: 03	ISE II:	15 Marks
	ISE III:	10 Marks
	End Semester Ex	am: 60 Marks

**Course description**: This course covers the fundamentals of digital communication. It deals with pulse modulation and digital modulation techniques. It also covers interference in transmission and probability of error in received signal. Spread Spectrum Modulation is dealt with appropriately.

# **Course Objectives:**

- Understand the fundamentals of digital communication.
- To explain about the pulse modulation and digital modulation techniques
- To make students aware of interference in digital modulated signal
- To give exposure to Spread Spectrum Modulation

#### **Course Outcomes:**

After completing the course, students will be able to:

CO1	Define basic concepts of pulse modulation, digital modulation, spread spectrum	K1
	modulation	
CO2	Explain various types of pulse and digital modulation and demodulation techniques	K2
CO3	Formulate mathematical representation of pulse, digital modulation -demodulation	K3
CO4	Describe the significance of noise in digital communication systems	K2
CO5	Understand the spread spectrum of modulated signal	K2
CO6	Interpret the performance of pulse and digital modulation techniques	K3

# **Detailed Syllabus:**

Unit 1	Pulse modulation: Sampling, Quantization, Pulse code modulation, line coding, T1
	Digital System, DPCM, DM, ADM, Voice coder (Vocoders)
Unit 2	Digital Modulation Techniques: Phase shift keying, Quadrature Amplitude shift keying,
	Frequency shift keying, Pulse shaping, reduction of inter channel and inter symbol
	interference, regenerative repeaters.
Unit 3	Optimal Reception of Digital Signal: Baseband signal receiver, probability of error,
	optimum receiver for both baseband and pass band, optimal coherent reception: PSK,
	FSK, QPSK. Signal space representation and Comparison of modulation system.
Unit 4	Noise in PCM and DM, PCM Transmission, Delta Modulation Transmission,
	Comparison of PCM and DM, The space shuttle ADM
Unit 5	Spread Spectrum Modulation: Spread Spectrum, Pseudo noise Sequences, DSSS, FHSS
	and Code Division Multiple Access Ranging

# Text books and Reference books

- H. Taub and D. L. Schilling, "Principles of Communication Systems", 3<sup>rd</sup> Ed, McGraw-Hill 2012
- 2. Simon Haykin, "Digital Communications", John-Wiley, 4<sup>th</sup> Ed , 2006

- 3. B. Carlson, "Communication Systems: An Introduction to Signals and Noise in Electrical Communication", 5th Ed, McGraw-Hill,2010
- K S Shanmugam, "Digital and Analog Communication Systems", John-Wiley & Son,2006
   R P Singh and S D Sapre, "Communication Systems ",2<sup>nd</sup> Ed, McGraw-Hill,2007

Course	PO	PS	PS	PS											
Outcome	1	2	3	4	5	6	7	8	9	10	11	12	01	O2	03
CO1	1	1	1											3	
CO2	2	2	1		1					2				3	
CO3	3	3	2		2									3	1
CO4	2	2	2		1					2				3	
CO5	2	2	2			1	1	2		2				3	
CO6	3	2	2		2									3	1

Mapping of Course outcome with Program Outcomes and Program Specific Outcomes

#### 3–High 2 – Medium 1 – Low

# Assessment:

ISE I:	Shall be based on Class Tests/ Assignments/ Quizzes/ Field visits/ Presentations/ Course Projects
ISE II:	Shall be based on class test
ISE III:	Shall be based on Class Tests/ Assignments/ Quizzes/ Field visits/ Presentations/ Course Projects

# **Assessment Pattern:**

Level No.	Knowledge Level	ISE I	ISE II	ISE III	End Semester Examination
K1	Remember	05	00	00	06
K2	Understand	10	05	05	42
K3	Apply	00	10	05	12
K4	Analyze	00	00	00	00
K5	Evaluate	00	00	00	00
K6	Create	00	00	00	00
Total Marks	100	15	15	10	60

#### **Assessment table**

Assessment Tool	K1	K2	K3	K2	K2	K3
	CO1	CO2	CO3	CO4	CO5	CO6
ISE I (15) Marks)	05	10	00	00	00	00
ISE II (15 Marks)	00	05	10	00	00	00
ISE III (10 Marks)	00	00	05	00	05	00
ESE Assessment (60 Marks)	06	24	06	12	06	06

ETPC3021: Lab Digital Communication				
Teaching Scheme	Examination Scheme:			
Practical: 2 Hrs/Week	ISE III: 25 Marks			
	Practical Examination & Viva Voce: 25 Marks			

# **Course Outcomes:**

After completing the course, students will be able to:

CO1	Perform various pulse modulation and demodulation techniques	<b>S</b> 1
CO2	Perform various digital modulation and demodulation techniques	S2
CO3	Interpret the performance of modulation techniques in presence of noise	S2
CO4	Use modern tools for simulation for modulation	<b>S</b> 2

# List of Experiments

1.	Study various Line coding techniques
2.	Perform PAM,PWM,PPM
3.	Perform Time DivisionModulation and demonstrate interlacing of at least three waveforms
4.	Perform Pulse Code Modulation and Demodulation and recover original signal
5.	Perform Delta and Adaptive Modulation and Demodulation. Observe change of step size in ADM
6.	Perform Amplitude Shift Keying transmission and reception
7.	Perform Frequency Shift Keying transmission and reception. Find out bandwidth of modulated signal
8.	Perform Phase Shift Keying transmission and reception. Find out bandwidth of modulated signal
9.	Compare performance of digital modulation techniques by EYE diagram
10	Simulate Spread Spectrum modulation technique

# Mapping of Course outcome with Program Outcomes

Course	PO	PO	РО	PO	PO5	PO	PS	PS	PS						
Outcome	1	2	3	4		6	7	8	9	10	11	12	01	O2	O3
CO1	1	1		3	2					1				3	
CO2	1	1		2	2					1				3	
CO3	2	2		2	2					1				3	
CO4				2	3					1				3	
3 –High	2 - 1	Medi	um	<b>1-</b>	Low										

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#### **Assessment Table**

Assessment Tool	<b>S</b> 1	<b>S</b> 2	S2	S2
	CO1	CO2	CO3	CO4
ISE III (25 Marks)	03	12	05	05
Practical Examination & Viva Voce (25 Marks)	05	12	04	04

# **Assessment Pattern**

Level No.	SkillLevel	ISE III	Practical Exam
			and viva-voce
<b>S</b> 1	Imitation	03	05
S2	Manipulation	22	20
S3	Precision	00	00
S4	Articulation	00	00
S5	Naturalization	00	00
Total		25	25

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ETPC3022: Embedded Systems				
Teaching Scheme   Examination Scheme				
Lectures: 3Hrs/week	ISE I: 15 Marks			
Total credits: 03	ISE II: 15 Marks			
	ISE III: 10 Marks			
	End Semester Examination: 60 Marks			

#### **Course description**:

This course introduces the concept of Embedded System, Embedded Microprocessor and its peripherals, interrupts and exceptions, C/ Assembly Programming, Tool Chains, Emulation and Debugging. The course focuses on ARM RISC processors for embedded applications.

#### **Course Objectives:**

- To develop understanding about requirements and general design methodology of Embedded Systems.
- To apply hardware and software knowledge for developing Embedded Systems as per requirements, specifications, and constraints.
- To impart knowledge of serial communication protocols, ARM architecture and Real Time Operating Systems.
- To expose the students to recent trends of Embedded System.

#### Course Outcomes: After completing the course, the students will be able to:

CO1	Understand classification, design issues & metrics of embedded systems						
CO2	Comprehend ARM Basics, ARM architecture, instruction set, assembly k						
	language programmingand on-board devices						
CO3	Know serial communication protocols						
CO4	Interface different peripherals to ARM processor for engineering solutions K						
CO5	Understand real time systems and System-on chip concepts						
CO6	Design Embedded systems for various applications						

#### **Detailed Syllabus:**

Unit 1	<b>Introduction to Embedded Systems</b> Definition of Embedded System, Components of a typical Embedded System, classification, Characteristics, Design Metrics, Overview of Embedded. Processor technology, IC Technology, Design Technology, Hardware components like Microcontroller, GPP, ASSP, ASIP, SoC, Introduction to Real Time non-OS and RTOS systems
Unit 2	ARM as Embedded Processor ARM/RISC Design Philosophy, Introduction to ARM processors and its versions, ARM7/ARM9/ ARM11 features, advantages & suitability in embedded application, ARM7 Architecture, differentiation in Cortex Series (A, M, R), data flow model, programmers model, ARM Basics- Register, Stack, Processor modes, System Control Block, Interrupts and Exception Handling, Memory map, GPIO and ARM and Thumb instruction Set

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Unit 3	Communication Interfaces and on-cnip devices
	Introduction to Serial / Parallel Communication, SPI, I2C, RS232 Serial Port, CAN, USB.
	LPC 2148: Timer/Counter, Watchdog Timer, PWM, ADC, DAC
Unit 4	Embedded System Development
	ARM Assembly Language Programming using Keil, Interfacing of peripherals and
	programming. Embedded system applications: Home Automation, vending machine or any
	other
Unit 5	System on Chip
	Introduction to Zvng SoC. Anatomy of Embedded SoC. IP block design. High Level
	Synthesis, Case Study- Video Processing and Computer Vision on Zyng
Text a	nd Reference Books
1 CAL a.	ADM System Developer's Chide Andrew N. Sloss Dominic Sympos. Chris Wright
1.	ARM System Developer's Guide, Andrew N. Sloss, Dominic Symes, Chris wright,
	ELSEVIER, 2005, ISBN 81814/6468, 97881814/6463
2.	ARM System-On-Chip Architecture, 2 <sup>ND</sup> ED, Steve Furber, Pearson Education, 2007, ISBN
	8131708403
3.	Embedded Systems Design, 2 <sup>™</sup> ED, Steve Heath, Newnes, 2003, ISBN 0750655461
4.	Professional Embedded ARM Development, James A. Langbridge, John Wiley & Sons, Inc.,
	2014, ISBN 9781118788943
5.	The Zyng Book, 1 <sup>st</sup> ED, Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, RobertW.
	Stewart, Strathclyde Academic Media, 2014
6.	ARM Assembly Language Fundamentals and Techniques, 2 <sup>ND</sup> ED, William Hohl, Christopher
	Hinds, CRC Press, 2015, ISBN 9781482229868
7.	ARM Assembly Language with Hardware Experiments. Ata Elahi, Trevor Arieski, Springer,
	2014 ISBN 9783319117034
8	PCL System Architecture 4 <sup>TH</sup> ED Tom Shanley Don Anderson MindShare Inc PEARSON
0.	Education 2006 ISBN 813170100X
	Education, 2000, ISBN 0151701007

# Mapping of Course Outcome with Program Outcomes and Program Specific Outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	1	1							1	1	1		1		
CO2	2	2	1						1	1	1	1		2	
CO3	3	2	1	1	1				1	1	1	1	2		
CO4	2	2	2	2	2				1	1	1	2			2
CO5	2	2	1	1	1				1	1	2	1	2		
CO6	2	2	2	2	2				2	2	3	2	2		2

**3- High 2-Medium 1-Low** 

#### Assessment:

ISE I:	Shall be based on Class Tests/ Assignments/ Quizzes/ Field visits/ Presentations/ Course Projects
ISE II:	Shall be based on class test
ISE III:	Shall be based on Class Tests/ Assignments/ Quizzes/ Field visits/ Presentations/ Course Projects

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#### **Assessment Pattern**

Level No.	Knowledge Level	ISE I	ISE II	ISE III	End Semester Examination
K1	Remember	03	03	00	06
K2	Understand	12	12	00	36
K3	Apply	00	00	10	18
K4	Analyze	00	00	00	00
K5	Evaluate	00	00	00	00
K6	Create	00	00	00	00
Total Marks 100		15	15	10	60

# Assessment Table

Assessment Tool	K2	K2	K2	K3	K2	K3
	CO1	CO2	CO3	CO4	CO5	CO6
ISE I (15 Marks)	10	05	00	00	00	00
ISE II (15 Marks)	00	10	05	00	00	00
ISE III (10 Marks)	00	00	00	05	00	05
ESE Assessment (60 Marks)	12	18	06	12	06	06

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ETPC3023: Lab Embedded Systems							
Teaching Scheme	Examination Scheme						
Practical: 2 Hrs/Week	ISE III: 25 Marks						
	End Semester Examination:	25 Marks					

# Laboratory Course Outcomes

As an outcome of completing the Laboratory course, students will be able to:

CO1	Use modern engineering tools necessary for integrating software and hardware							
	components in Embedded system designs.							
CO2	Write programs in assembly language programming for ARM processor							
CO3	Program the basic interfacing of ARM processor with peripherals using Embedded C							
CO4	Demonstrate the data communication using SPI/ I2C and exception handling with ARM							
	processor							

# List of Experiments (Any 8)

Sr. No.	List of Experiments
1	Practice IDE software and universal programmer to program microcontrollers.
2	ARM Instruction set and Assembly language programming 1
3	Program to Interface LEDs to LPC2148 for generating patterns
4	Program to Interface Seven Segment display
5	Program to Interface keys/ key matrix
6	Program to Interface LCD/Graphics LCD
7	Program to Interface Buzzer, relay
8	Program to Interface ADC/DAC
9	Program to Interface Stepper motor/ temperature sensor
10	Use external interrupt to carry out ISR
11	Data communication using SPI/I2C
12	Understand free RTOS tutorial

#### Mapping of Course outcome with Program Outcomes and Program Specific Outcomes

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Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO11	PO 12	PSO1	PSO2	PS03
Outcome															
CO1	1	2		1	1					1			2		
CO2	1	2		1	2				2	1			3		
CO3	1	2		2	2				2	1			3	2	2
CO4	2	2		2	2					2			3	2	2

3 – High2 – Medium 1 - Low

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#### **Assessment Table**

Assessment Tool	<b>S</b> 1	S2	S2	S2
	CO1	CO2	CO3	CO4
ISE III (25 Marks)	03	14	04	04
ESE (25 Marks)	05	12	04	04

#### Assessment Pattern

Level No.	Skill Level	ISE III	ESE
S1	Imitation	03	05
S2	Manipulation	22	20
S3	Precision	00	00
S4	Articulation	00	00
S5	Naturalization	00	00
Total		25	25



ETPR3001: Mini-Project I						
Teaching Scheme	Examination Scheme					
Lectures: 2 Hrs/Week	ISE III:25 marks					
Credits: 01	Practical /Viva-voce:25 marks					

**Course description**: The aim of this course is to enable the student to comprehend the principles of modern manufacturing processes / software and to acquire competency in the design, construction, and documentation of electronic equipment/ algorithms.

#### **Course Objectives:**

- Elaborate the design processes and production methods.
- Explain the use of software techniques and thermal analysis techniques.

#### **Course Outcomes**

After completing the course, students will be able to:

CO1	Identify task and required circuit diagram / system for it.
CO2	Build a project model, simulate, and test it through software.
CO3	Demonstrate working of the project.

#### **Detailed Syllabus:**

A group of three or four students shall select a topic from the field of Electronics and Telecommunication Engineering. They have to build a system / mini project / algorithm and test it.

Term Work: It will consist of a report based on the study and actual work done on the selected topic, which will cover theoretical and analytical study of the system, specifications, applications, results etc.

Students are expected to design an IC based project of analogue / digital circuit / software system (This can be used as experimental set-up in the laboratory). PCB design, fabrication, testing and implementation / flow charting, modular design etc. should be done. Students may use the software simulation for verification of hardware implementation. Documentation of the project is to be in standard IEEE format. Project report should include abstract in 100 words (max), key words, introduction, design, simulation, implementation, results/ results comparison, conclusion and references.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO 1	PSO 2	PSO 3
CO															
CO1				2	3										
CO2	3	1													
CO3	1		2	3											

3 – High 2 – Medium 1 - Low

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#### **Assessment Pattern**

Level	Knowledge Level	ISE III	Practical Viva – Voce
<u>S1</u>	Imitation	05	05
S1 S2	Manipulation	15	15
S3	Precision	05	05
S4	Articulation	00	00
S5	Naturalization	00	00
S1	Imitation	25	25

### Assessment table:

Assessment Tool	<b>S1</b>	<b>S2</b>	<b>S3</b>	
	CO1	CO2	CO3	
ISE III	05	05	15	
Practical / Viva-voce	05	05	15	

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