BIO-DATA

Name :ShitalBipinchandraGundre

Designation: Assistant Profesor

Experience: 6.5 Years

Educational Qualifications: M. E. (Electronics)

Ph.D. topic:NA

Recognized Ph.D. guide at:NA

Research Areas:Istrumentation, Embedded System

Research Project Completed:NO

Member of Professional Bodies: ISTE

Publications:

- **International Journal Papers:01**
- **International Conference:01**

Publications:

1) S. B. Gundre and G. S. Lipane, "Palm Print Recognition Review Paper",*International Journal of Engineering Trends and Technology*- Volume 4, Issue2- 2013.

2) S. B. Gundre and Sudhir K Ingole, " Characters Feature Based Indian Vehicle License Plate Detection and Recognition", IEEE sponsored 2017 International Conference on Intelligent Computing and Control, held on 23rd& 24th June 2017, Karpagam college of Enginnering, Coimbtore, India.

Short Term Training Programme Organized:

TEQIP"Signal & Image Processing" (SIP- 2017), scheduled during Feb 6th,2017 to Feb 10th , 2017, by E&TC Dept, Government College of Engineering, Aurangabad

Short Term Training Programmes Participated:

Sr.No	Details of FDP attended (including title of training, name of department and institute where training is attended)	Year
2	ISTE Skill Matrix Enhancement and effective Teaching Learning for quality technical education 28.11.2011 to 09.12.2011,Government College of Engineering, Aurangabad	2011
3	ISTE Engineering Optimization Techniques and its applications in Research 02.01.2012 to 12.01.2012 ,Government College of Engineering, Aurangabad	2012
	Analog System Design & MSP 430 Development Tools ,26.11.2012 to 30.11.2012,College of Engineering, Pune	2012
4	AICTE Embedded System Development using DSP's 20/5/2013 to 31/05/2013,College of Engineering Pune	2013
5	AICTE Advanced Power Electronics and Drives 09/12/2013 to 20/12/2013, Walchand College of Engineering Sangali	2013
6	Tarinig Program on OrCad Software 15/01/2013 to 19/01/2013 WINSpect Info-system Pvt. Ltd. ,Navi Mumbai and Government College of Engineering Aurangabad	2013
7	TEQIP System Design using FPGA 24/06/2013 to 28/06/2013, Government College of Engineering, Aurangabad	2013
8	TEQIP"Signal & Image Processing" (SIP- 2017), scheduled during Feb 6 th ,2017 to Feb 10 th , 2017, by ETC Dept, Government College of Engineering, Aurangabad	2017
9	ISTE "CMOS, MIXED SIGNAL AND RADIO FREQUENCY VLSI DESIGN " under MHRD NMEICT which is being organized in Marathwada Institute of Technology, Aurangabad, by IIT Kharagpur during Jan 30 , 2017 to Feb 04, 2017	2017
10	TEQIP"Optimization in Machine Learning" organized by IT Department GECA from 27th Feb to 3rd March 2017	2017